





A cross-sectional view of a semiconductor device. The device is built on a substrate 21. A P-type region 23 is formed on the substrate. A P+ region 30 is formed on the P-type region 23. An N+ region 26 is formed on the P+ region 30. A resistor 24 is formed on the N+ region 26. A Vdd connection 25 is formed on the resistor 24. A P- region 28 is formed on the P-type region 23. A P+ region 27 is formed on the P- region 28. A D region 22 is formed on the P+ region 30. A M1 layer 23 is formed on the P- region 28. A P+ region 26 is formed on the P+ region 30. A N+ region 24 is formed on the N+ region 26. A resistor 25 is formed on the N+ region 24. A Vdd connection 27 is formed on the resistor 25. A P- region 28 is formed on the P-type region 23. A P+ region 27 is formed on the P- region 28. A D region 22 is formed on the P+ region 30. A M1 layer 23 is formed on the P- region 28. A P+ region 26 is formed on the P+ region 30. A N+ region 24 is formed on the N+ region 26. A resistor 25 is formed on the N+ region 24. A Vdd connection 27 is formed on the resistor 25.

**FIG. 5**  
(PRIOR ART)

